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HSF Property:ROHS

ACER
JM31/SJM31/BAP31
Discrete
MAIN BOARD

2009.05.26

Tuesday, May 26, 2009		A03
DATE	CHANGE NO.	REV

	EE	DATE	POWER	DATE	INVENTEC			
DRAWER					TITLE BAP31G SFF			
DESIGN								
CHECK RESPONSIBLE								
SIZE=					VER:			
FILE NAME: XXXX.XXXXXX.XX					SIZE	CODE	DOC NUMBER	
PIN	XXXXXX000000				C	CS	D-CS-1310A2264501-ALG	REV
					SHEET	1	of	47

1. Schematic Page Description :

Montevina Schematic Ver : A03

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

30. ICH9M Power/GND(4/4)

31. LCD CNN/SATA/3G/WLAN

32. KBC ITE8512F

33. IO CN

34. IO CN

35. IO CN

36. Audio Codec

37. BLANK

38. M92-S2(1/5)

39. M92-S2(2/5)

40. M92-S2(3/5)

41. M92-S2(4/5)

42. M92-S2(5/5)

43. DDR3 VRAM

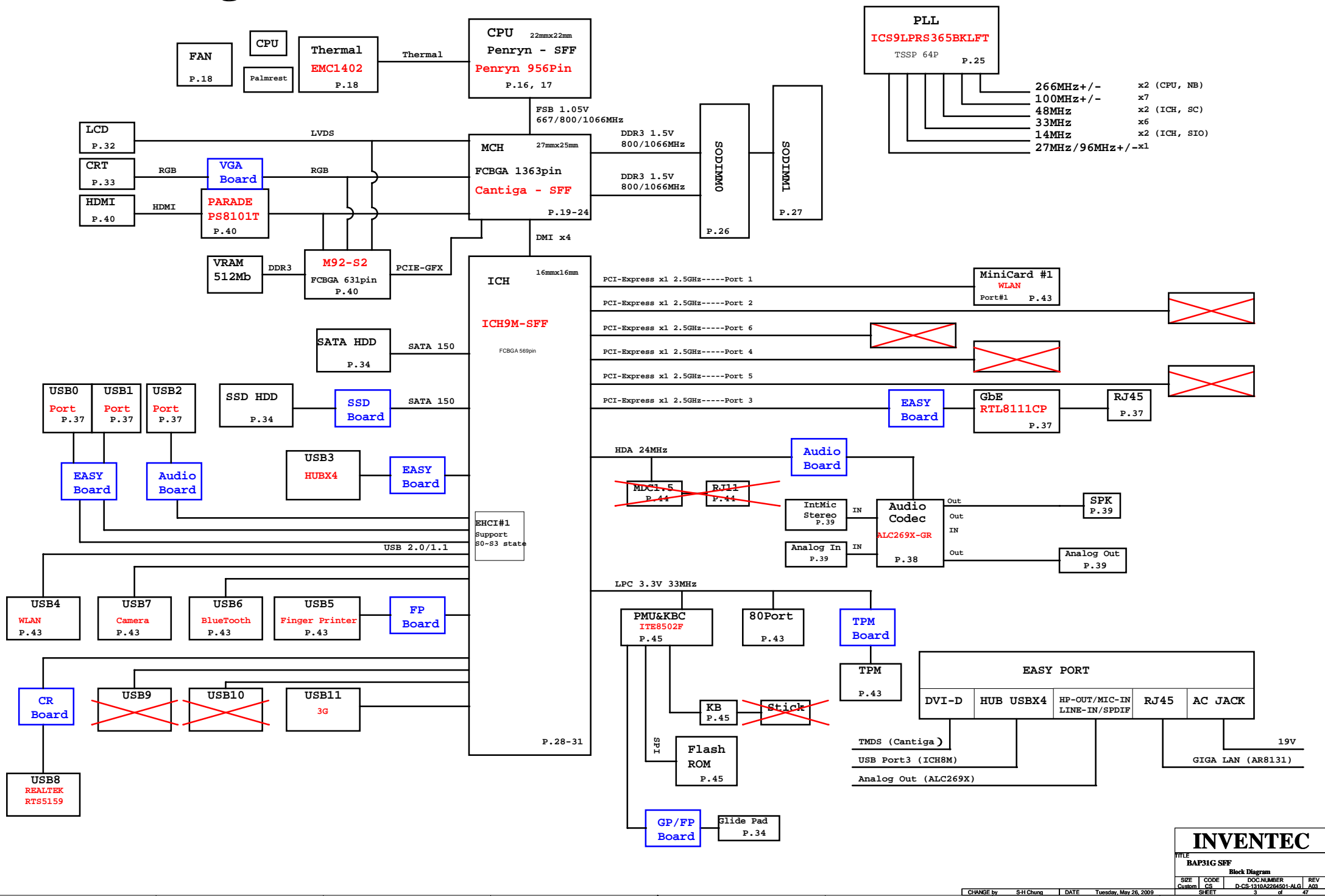
44. HyBrid Switch

45. dGPU Power

46. dGPU Power

47. dGPU Power

3. Block Diagram :



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
+5VA	5.0V always on power rail by ECPWON
+3VA	3.3V always on power rail by ECPWON
+5VS	5.0V switched power rail by SLP_S3#_3R
+3VS	3.3V switched power rail by SLP_S3#_3R
+1.8VS	1.8V switched power rail by SLP_S3#_3R
VCC_CORE	Core Voltage for CPU
+1.05VS	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
+1.25VS	1.25V switched power rail by SLP_S3#_3R
+1.5VS	1.5V power rail for CPU PLL/DMI/PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9m by SLP_S3#_3R
+1.5V	1.5V power rail for DDRII by SLP_S5#_3R
0.75VDDT_DDRIII	0.75V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer
Layer 4		Power Plane
Layer 5		Stripline Layer
Layer 6		Stripline Layer
Layer 7		Ground Plane
Layer 8		Solder Side, Microstrip signal Layer

	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	95 ohm +/- 20%	95 ohm +/- 20%
PCI-E Clock	95 ohm +/- 20%	95 ohm +/- 20%
DDR3 CLK	75 ohm +/- 20%	75 ohm +/- 20%
DDR3 Strobe	90 ohm +/- 20%	90 ohm +/- 20%
DMI Bus	95 ohm +/- 20%	95 ohm +/- 20%
PCIE Bus	95 ohm +/- 20%	95 ohm +/- 20%
SDVO	95 ohm +/- 20%	95 ohm +/- 20%
SATA	95 ohm +/- 20%	95 ohm +/- 20%
USB	90 ohm +/- 20%	90 ohm +/- 20%
LVDS	95 ohm +/- 20%	95 ohm +/- 20%
Lan	95 ohm +/- 20%	95 ohm +/- 20%

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Penryn SFF HFM: LFM:	1.3319V~1.4375V~1.4591V 0.9221V~0.9625V~0.9739V	18A
1.05VS	Penryn SFF : AGTL+ termination Cantiga GS: Core Cantiga GS: PCIE Cantiga GS:Core+IMEL+HSIO Cantiga GS:VCC_GMCH Cantiga GS:VCCA_SM_CK and NCTF Cantiga GS:VCC_DMI Cantiga GS:VCCA_SM Cantiga GS:VTT ICH9M:VCC1_05 ICH9M:DMI ICH9M:CPU_IO	1V~1.05V~1.10V 0.997V~1.05V~1.102V 0.9975V~1.05V~1.1025V 0.9975V~1.05V~1.1025V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V 0.997V~1.05V~1.102V	4.5A 8.7A 1.78A 2.898A 10.154A 37.95mA 456mA 747.5mA 852mA 1.634A 48mA 2mA
1.5VS	Penryn SFF PLL Cantiga GS: QDAC Cantiga GS: LVDS Cantiga GS: TVDAC Cantiga GS: Various PLLS analog supply Cantiga GS: VCC_SM_CK Cantiga GS: VCC_SM ICH9M:PCIE_ICH ICH9M:SATA_ICH ICH9M:VCC_GLAN Mini Card: Express Card:	1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.71V~1.8V~1.89V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V 1.425V~1.5V~1.575V	130mA 0.5mA 60.31mA 35mA 485mA 149.5mA 3.1625A 646mA 1.342A 80mA
1.5V	Cantiga GS: DDRIII System Memory	1.425V~1.5V~1.575V	3.1A(800M) 4.1A(1067M)
0.75VDDT_DDRIII	DDRIII Termination:	0.7125V~0.75V~0.7875V	1.0A
3VS	Cantiga GS: HV CMOS Cantiga GS: VCCS_TVDC ICH9M:VCC3_3 ICH9M:VCCGLAN3_3 Thermal Sensor: Mini Card: UMTS Express Card: CLK Generator: ICS9LPRS365BKLF Mini Card: WirelessLan Bluetooth: Super I/O: IT8305E Azalia Codec: ALC262 Azalia MDC:	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V	105.3mA 78mA 308mA 1mA 5mA 1.3A 500mA
1.8VS	DVI	3.0V~3.3V~3.6V	120mA
3VA	ICH9M: RTC ICH9M:VCCSUS3_3 ICH9M:VCCCL3_3 ICH9M:VCCLAN3_3 LCD: Lan:AR8131 Azalia MDC: Flash ROM: BIOS	2V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.135V~3.3V~3.465V 3.0V~3.3V~3.6V 3.0V~3.3V~3.6V	6uA 212mA 73mA 78mA 2A 1A
5VS	Cardreader: RTS5159 Azalia Codec: ALC269 HDD: SATA ODD: SATA Audio AMP: G1432 Inverter: WebCam	3.0V~3.3V~3.6V 3.0V~3.3V~3.6V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	Max: 1.5A ; R/W: 460mA ; STDBY: 70mA Max: 1.5A ; R/W: 900mA ; STDBY: 45mA
5VA	USB: x 2 ports USB	5VA 5VA	1A 2A 1.5A
5VLA	Control Power		
3VLA	EC: ITE8512E	3.0V~3.3V~3.6V	300mA

6.Schematic modify Item and History :

- 2009.0108
1. ADD USB P3 for Docking, USB P5 for Finger printer,
Modify CN5 -----P28

2. Modify CN20 to 50pin-----P33

3. Move PWR_SWIN# from CN14 to CN20

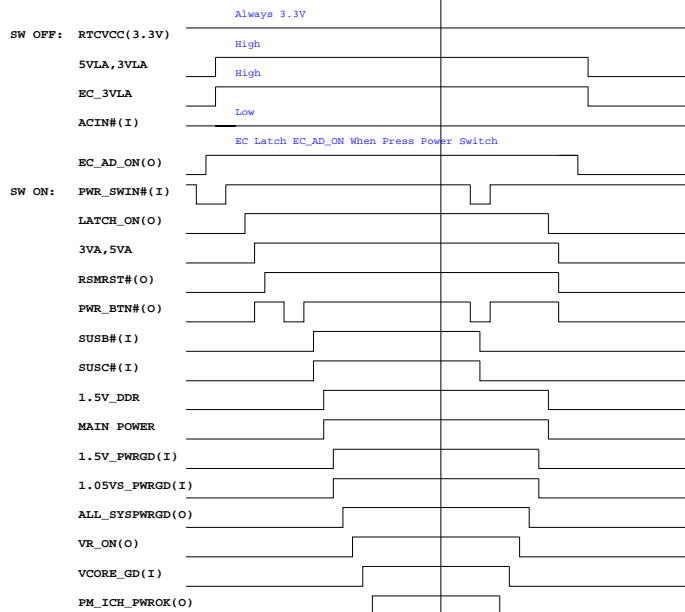
4. ADD TPM module-----P34
- 2009.0109
1. ADD DOCK_USB_EN, DOCK_CRT_IN#-----P32,33
- 2009.0112
1. Change power item: R490,R291,BAT CNN TH PIN

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang

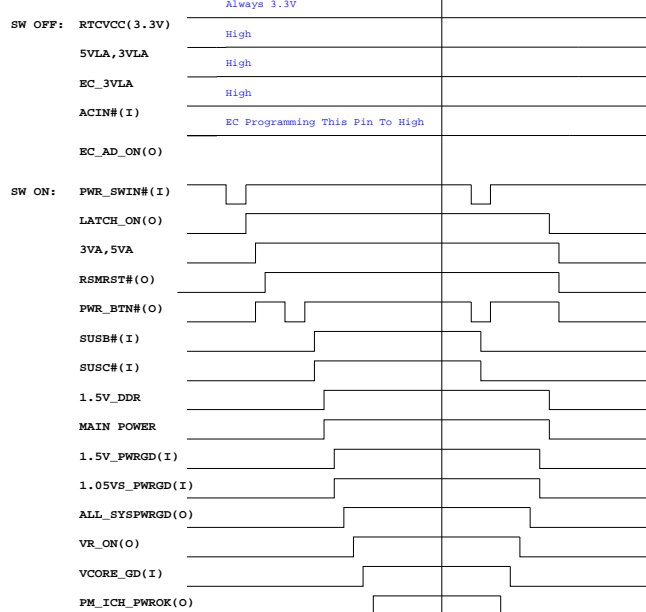
Power on/off sequence AC insert (without Battery Pack)

Power on sequence Power off sequence



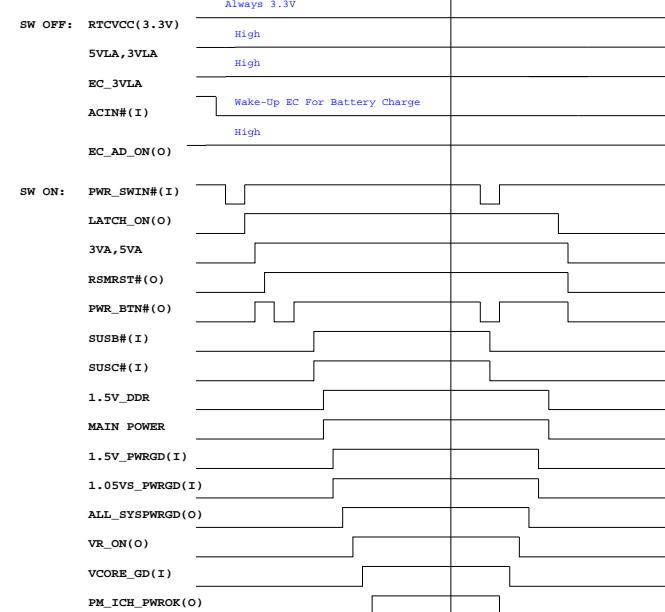
Power on/off sequence Battery insert (without AC adapter)

Power on sequence Power off sequence



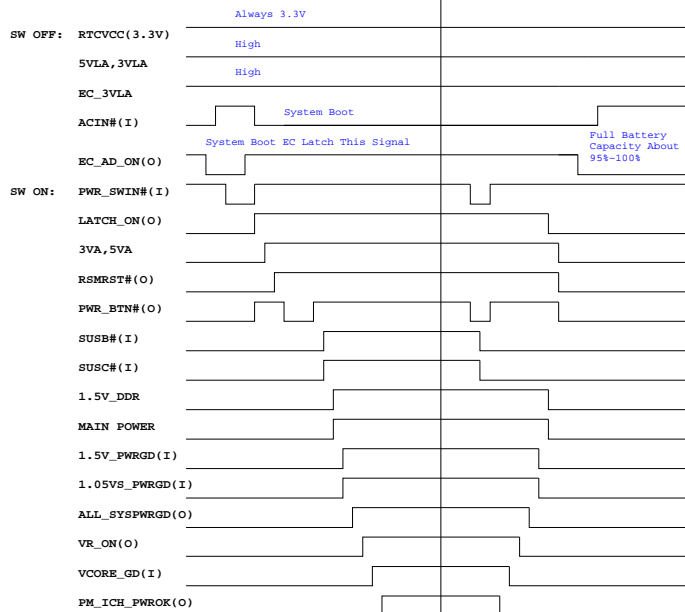
Power on/off sequence AC insert(with charge over 95%)

Power on sequence Power off sequence



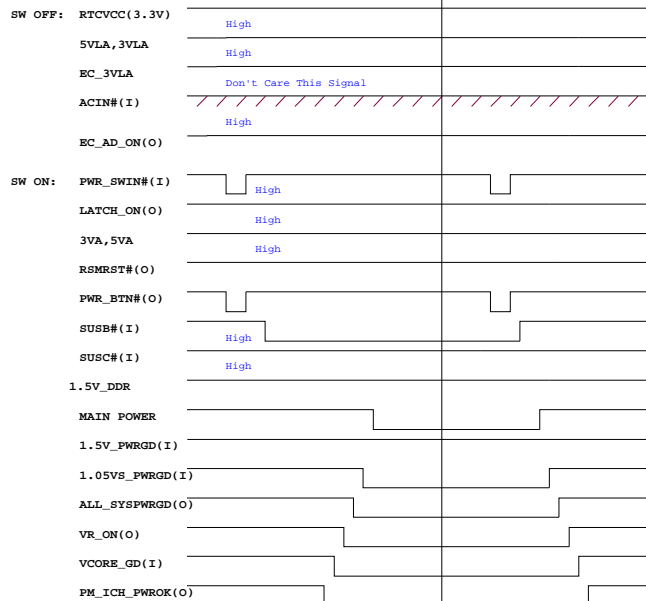
Power on/off sequence AC insert(without charge over 95%)

Power on sequence Power off sequence



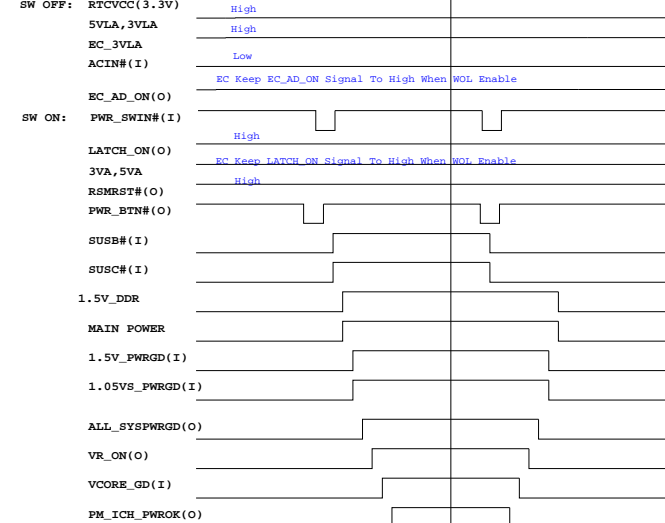
Suspend And Resume Sequence (S3)

Suspend sequence Resume sequence



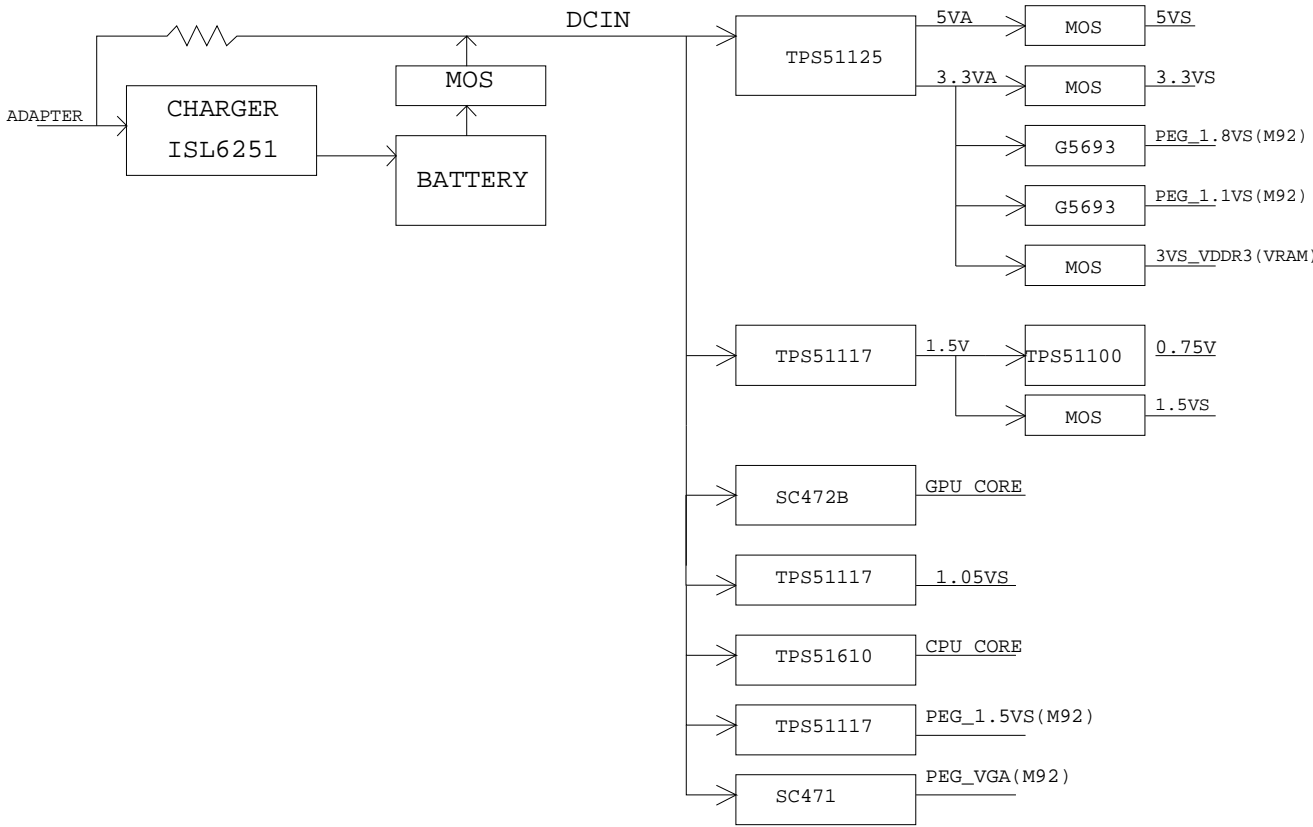
Power on/off sequence after windows shoutdown (WOL enable)

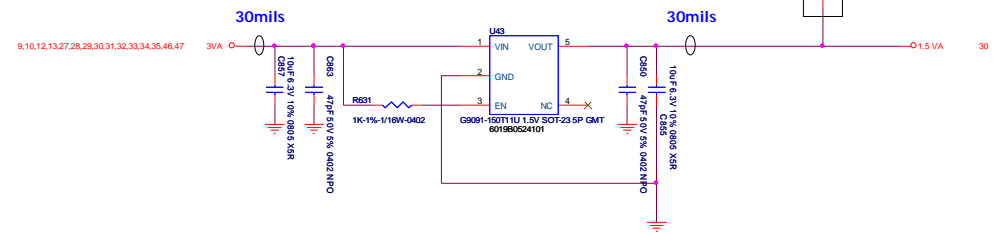
Suspend sequence Resume sequence



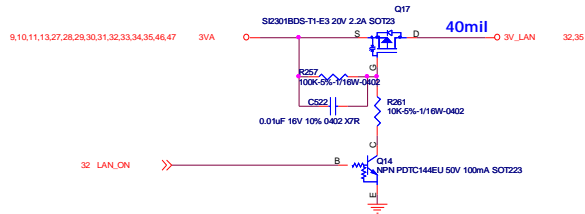
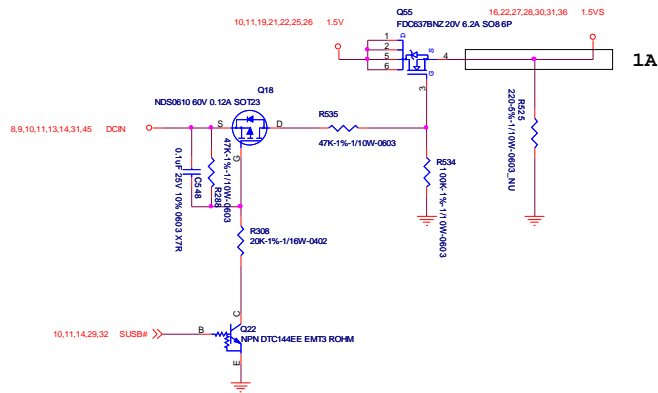
INVENTEC			
TITLE BAP31G SFF			
Time Diagram			
SIZE: Custom	CODE: CS	DOC NUMBER: DCS-1310A2264501-ALG	REV: A0
CHANGE by: S-H Chung		DATE: Tuesday, May 26, 2009	SHEET: 6 of 47

Power Block Diagram :

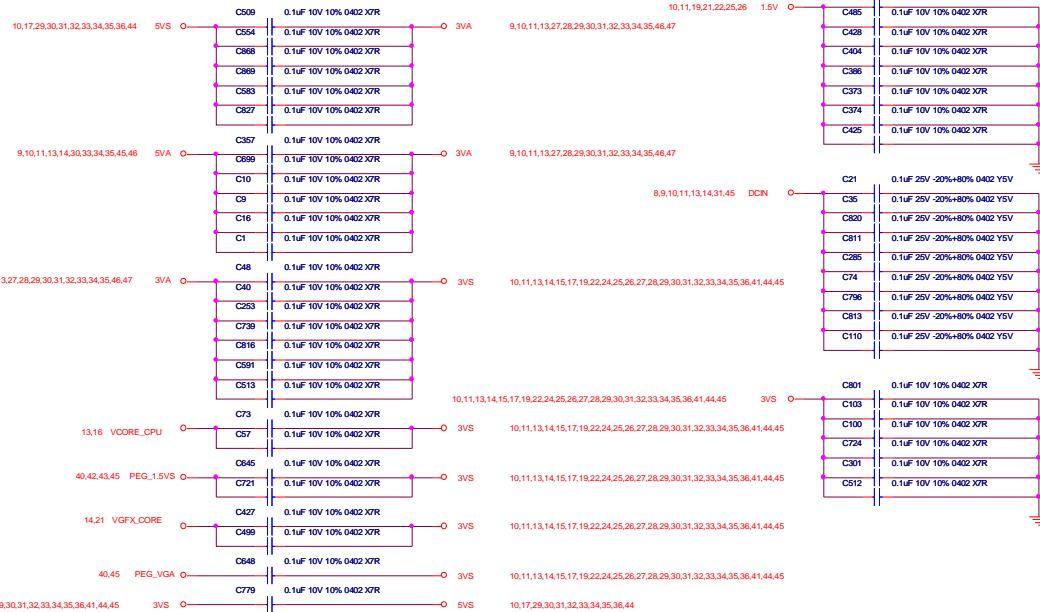




1.5VS

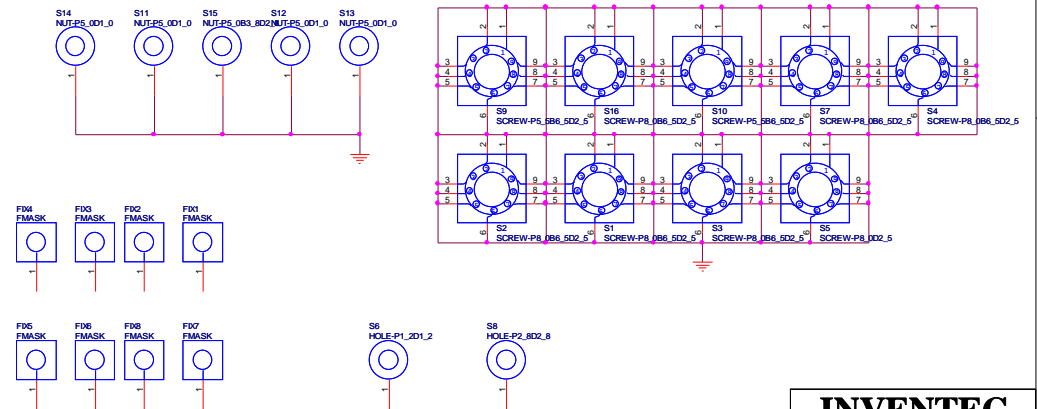
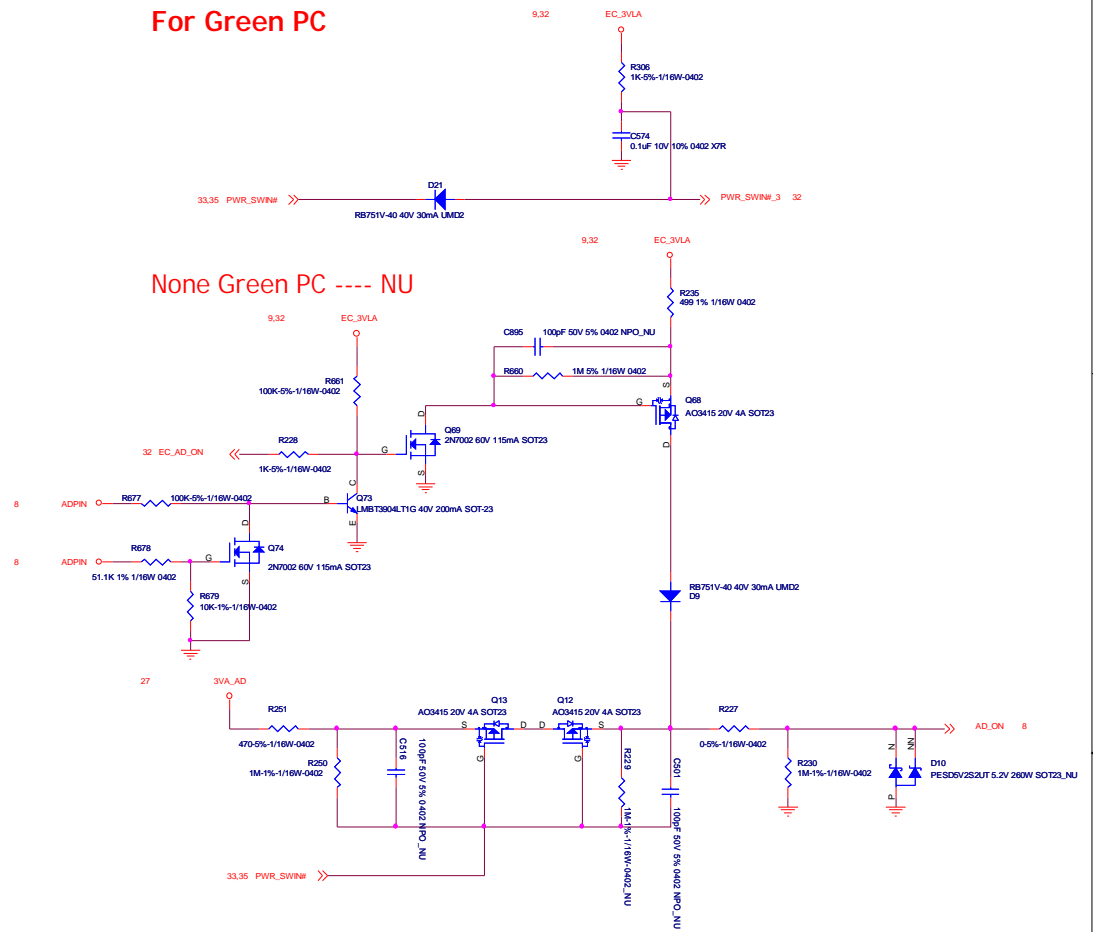


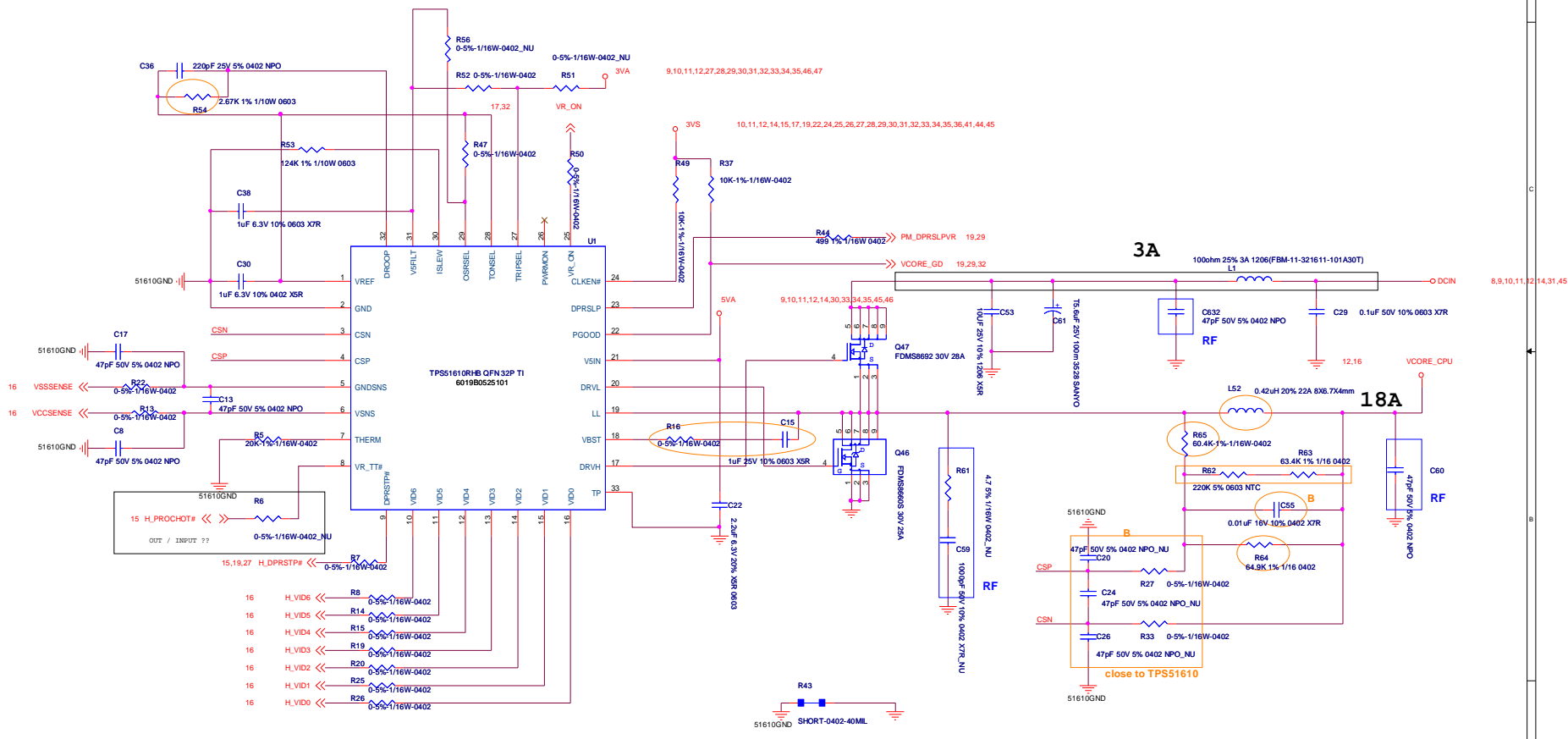
EMI Cap



For Green PC

None Green PC ---- NU





INVENTEC

FILE
BAP31G SFF

CPU Core Power

SHEET 13 of 47



XDP P/U & P/D

Signal	Pin	Value	Connection
XDP_DBRESET#	R88	1K-5% 1/16W-0402	3V5
XDP_TDO	R418	54.9-1% 1/16W-0402, NJ	1.06V5_CPU
XDP_TMS	R89	54.9-1% 1/16W-0402	
XDP_T0#	R419	54.9-1% 1/16W-0402	
XDP_BPM#5	R470	54.9-1% 1/16W-0402	
XDP_TRST#	R373	64.9-1% 1/16W-0402	
XDP_TCK	R405	54.9-1% 1/16W-0402	

— Should be connect to ICH9 and Cantiga without T-ing(no stub)

[illegible]

Comp0,2 connect with $Z_0=27.4\Omega$, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with $Z_0=55\Omega$, make trace length shorter than 0.5" and width is 5mils

ULV Dual-Core : 18A(max)
ULV Single-Core : 9A(max)

Power-up peak current : 4.5A (max)
Steady-state current : 2.5A (max)

Place these inside socket cavity on L8
(North side secondary)

Place these inside socket cavity on L8
(South side secondary)

Place these inside socket cavity on L1
(North side Primary)

Place these inside socket cavity on L1
(South side Primary)

North side secondary

South side secondary

Route VCCSENSE and VSSSENSE traces
at 27.4 ohms. Place PU and PD within
2 inch of CPU

Place these inside socket cavity on L8
(North side secondary)

160mil

Intel item 6

Close to CPU
pin B34

Impedance 55 Ohm, W:S= 1:2

Mismatch 25mil

18mil
7mil space
25mil space with other

CPU Penryn_SFF FCBGA 956P INTEL

INVENTEC

BAP31G SFF

Penryn Processor(2/2)

SIZE CODE DOCNUMBER
Custom CS D-CS-1310A2264591-ALG_A03

SHEET 16 of 47

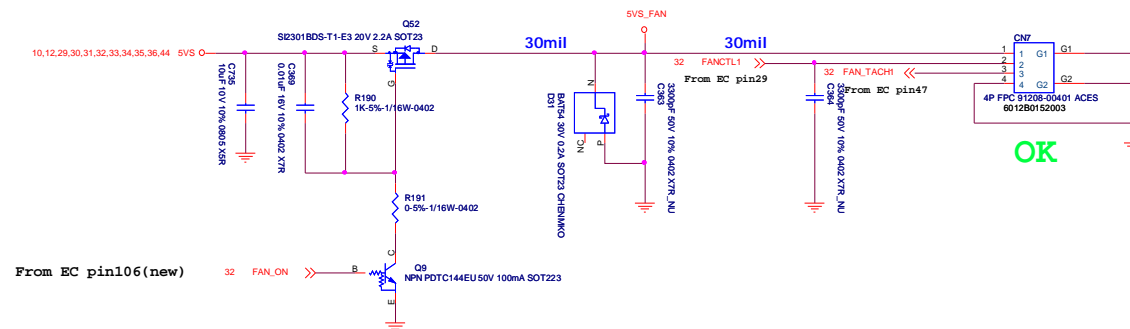
CHANGE by S-H Chung

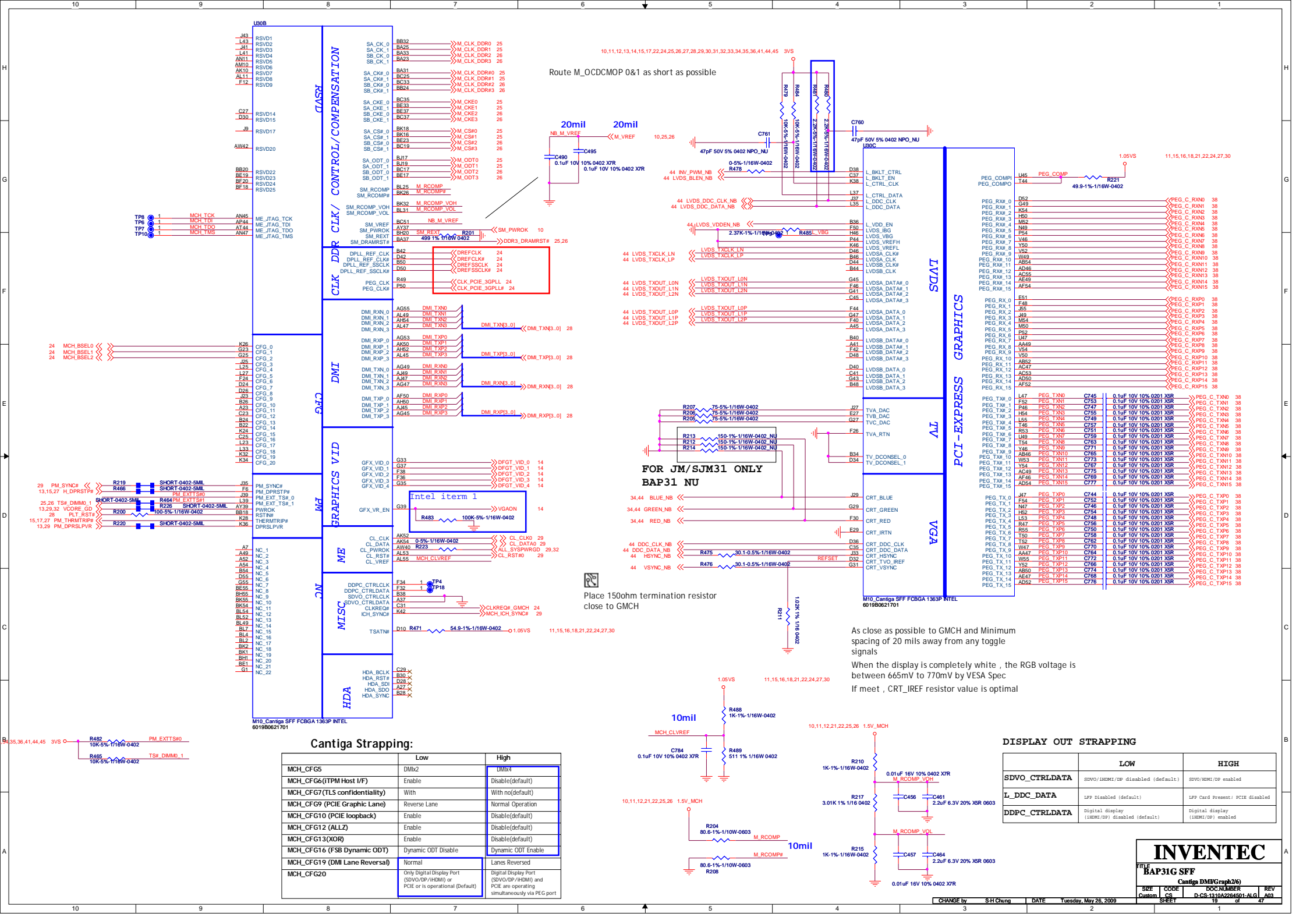
DATE Tuesday, May 26, 2009

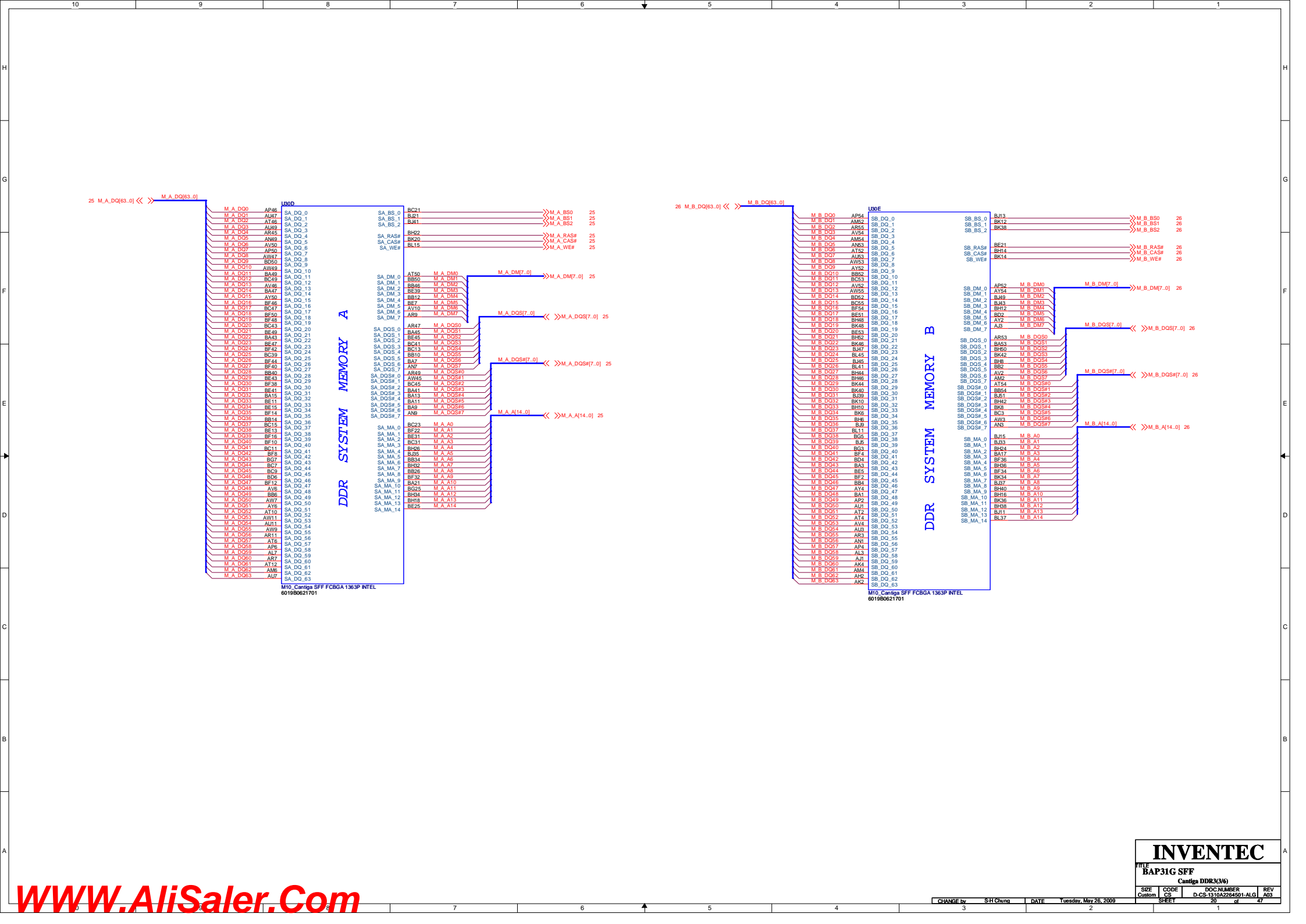
THERMAL SENSOR



Fan control



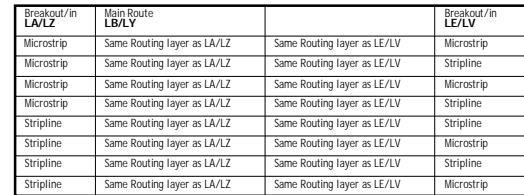




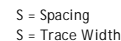



```

graph LR
    subgraph SMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ICH8m
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --> LA1[LA1]
    LA1 --> LA2[LA2]
    LA2 --> LB[LB]
    LB --> LC[LC]
    LC --> LD[LD]
    LD --> LE[LE]
    LE --> Rx2
    Tx2 --> LV[LV]
    LV --> LW[LW]
    LW --> LX[LX]
    LX --> LY[LY]
    LY --> LZ2[LZ2]
    LZ2 --> LZ1[LZ1]
    LZ1 --> Rx1
  
```

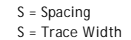
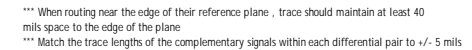


*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils

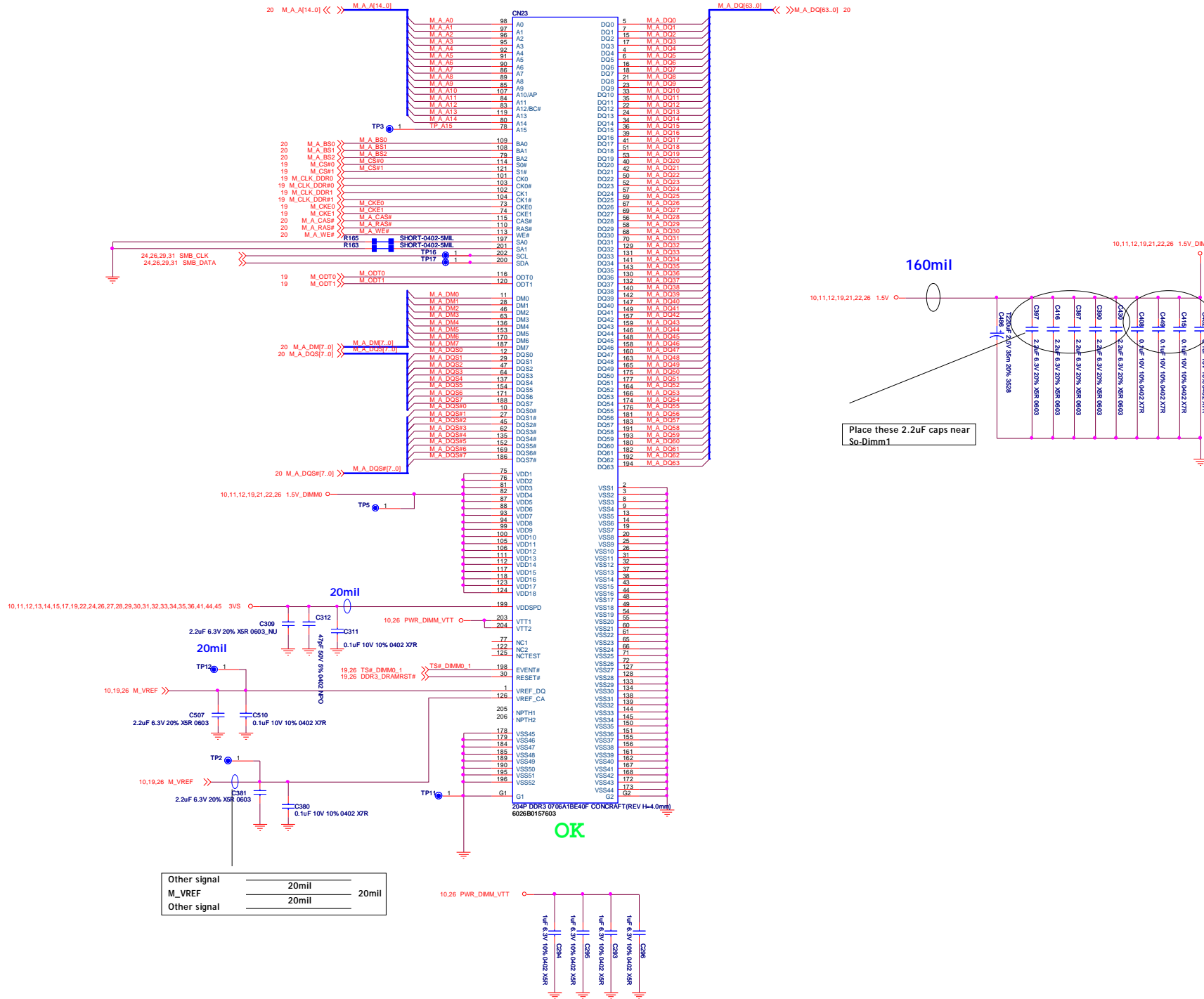


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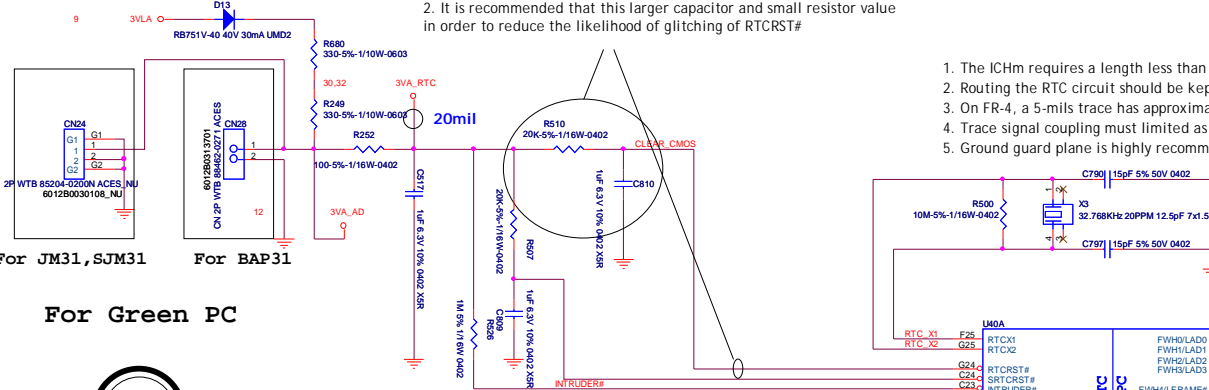
graph LR
    subgraph GMCH
        Tx1[Tx]
        Rx1[Rx]
    end
    subgraph ExpressMiniCard [Express/Mini Card]
        Rx2[Rx]
        Tx2[Tx]
    end
    Tx1 --- LA --- LB --- LC --- Rx2
    Rx1 --- LZ --- LY --- Tx2
    style LB stroke-dasharray: 5 5
    style LC stroke-dasharray: 5 5
  
```



SO-DIMMO



1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTRST#



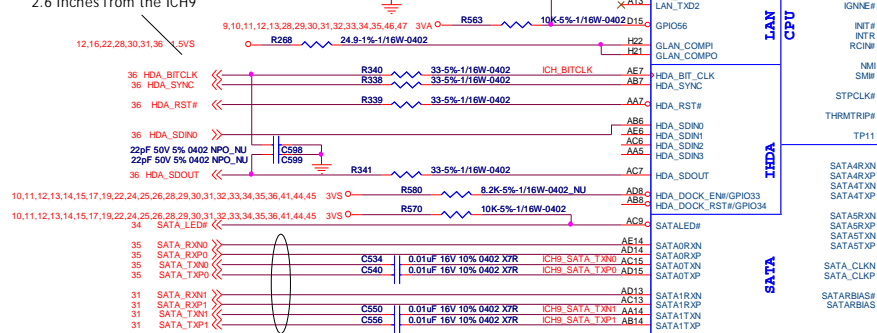
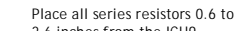
1. The ICHM requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

For Green PC

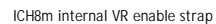


CABLE,ROUND,3POS,75mm,I,RTC_NU
6027B0066801

RTC Battery Life :
 $220\text{mAh}(220000\mu\text{Ah}) / 6\mu\text{A} = 4.2 \text{ year}$

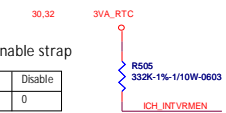


Distance between the ICH9-M and cap on the "P" signal should be identical distance between the ICH9-M and cap on the "N" signal for same pair.

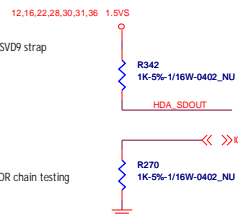


	Enable	Disable
INTVRMEN	1(Default)	0

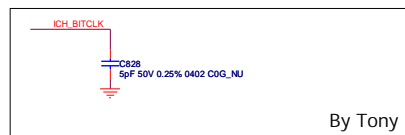
Internal VRM enabled for
VccSus1_05, VccSus1_5,
VccCL1_5, VccLAN1_05 and
VccCL1_05



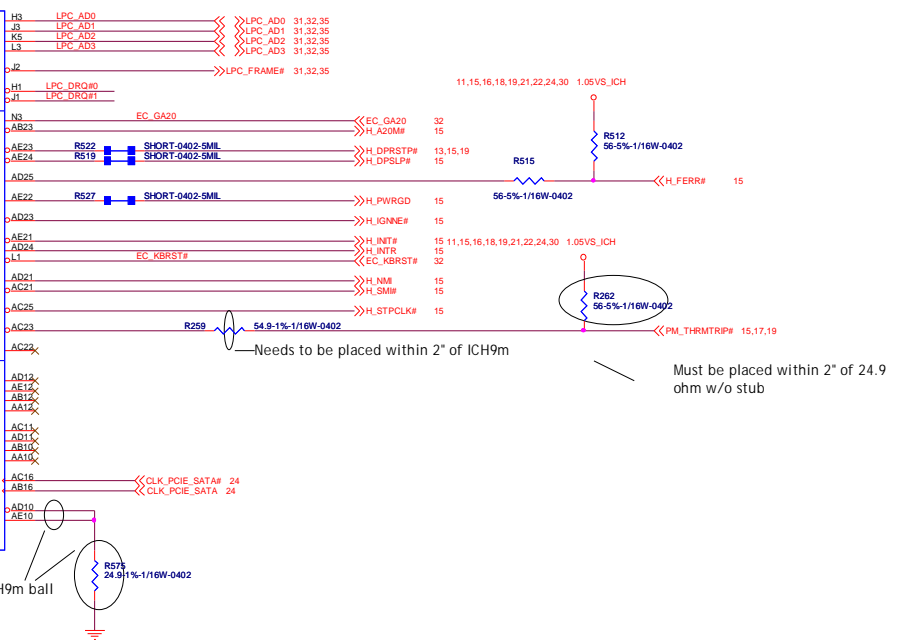
ACZ_SDATAOUT strap functionality base on RSVD9 strap
XOR chain entrance (RSVD9 pulled low)
PCIE port config bit 1(RSVD9 not pulled low)



XOR Chain Entrance Strap - to be updated		
ICH_TP3	HDA_SDOUT	Description
0	0	ESVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



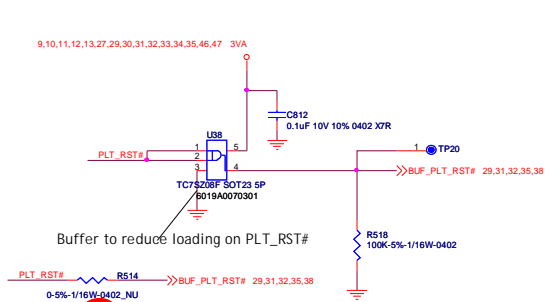
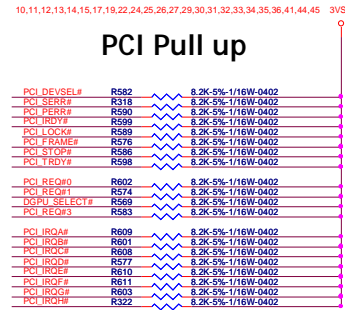
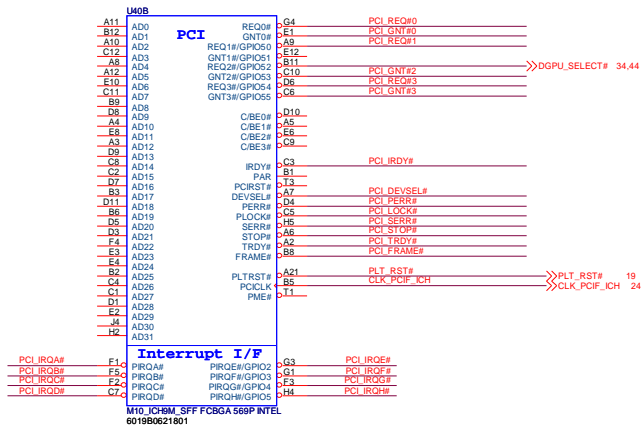
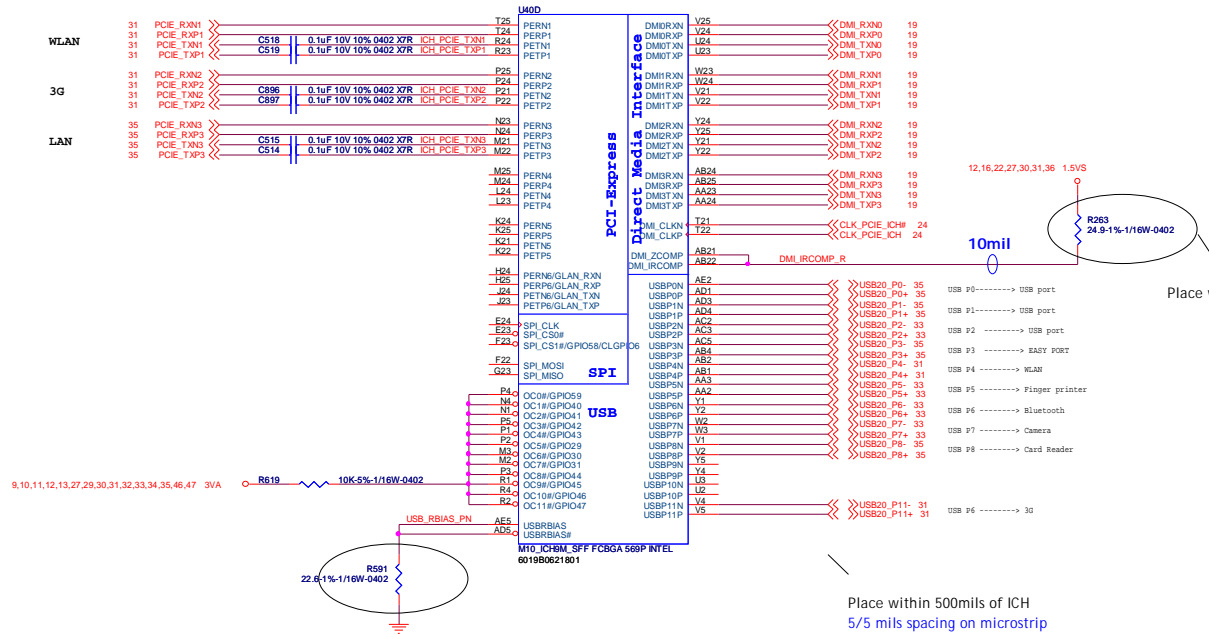
By Tony



U—Needs to be placed within 2" of ICH9m

Must be placed within 2" of 24.9
ohm w/o stub

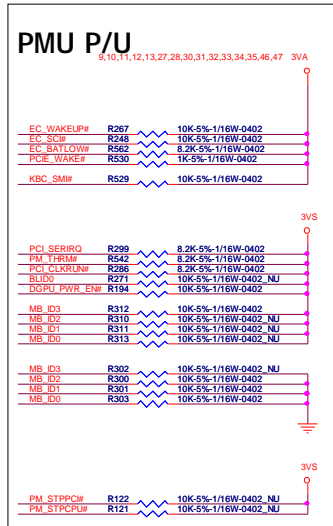
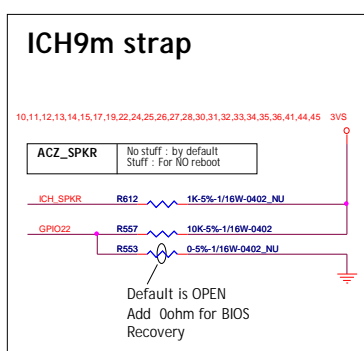
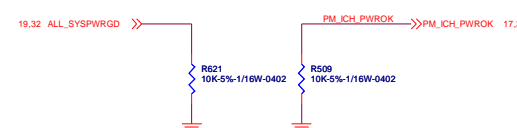
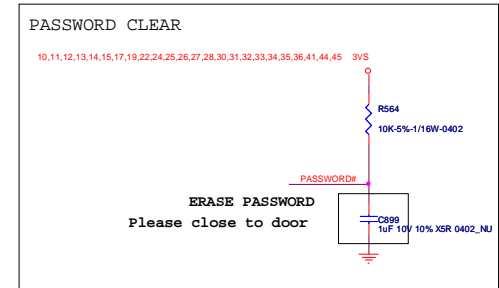
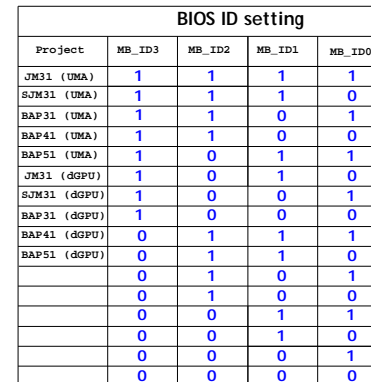
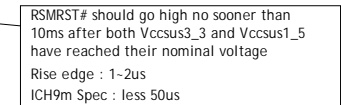
PCIE AC coupling caps need to be within 250mils of the driver



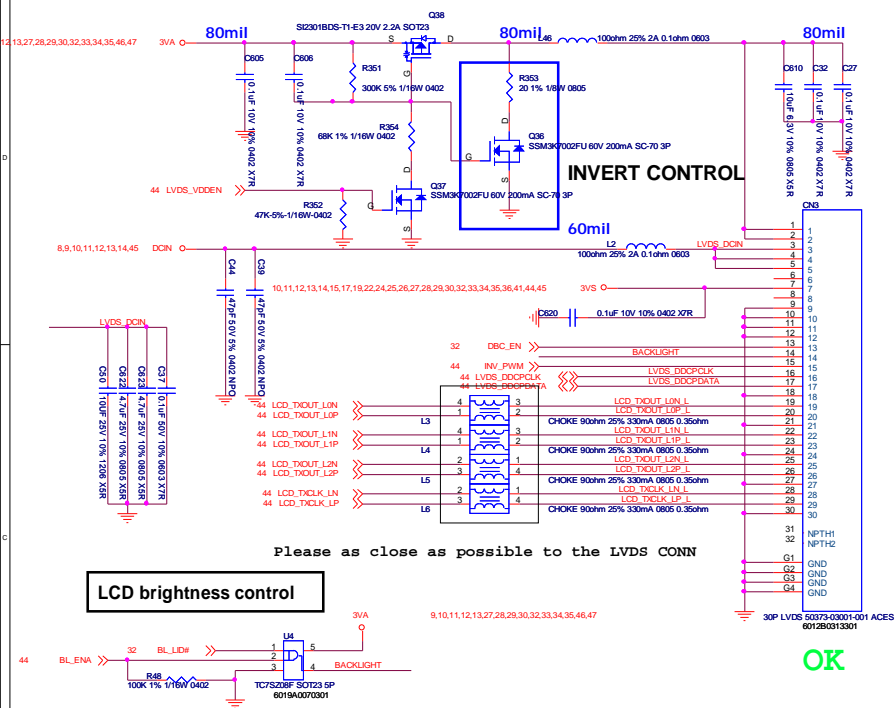
PCI_GNT#2	R573	1K-5%-1/16W-0402	NU
PCI_GNT#3	R567	1K-5%-1/16W-0402	NU
PCI_GNT#0	R604	1K-5%-1/16W-0402	NU

PCI_GNT#0	SPI_CS1#	LPC
1	1	LPC
1	0	PCI
0	1	SPI

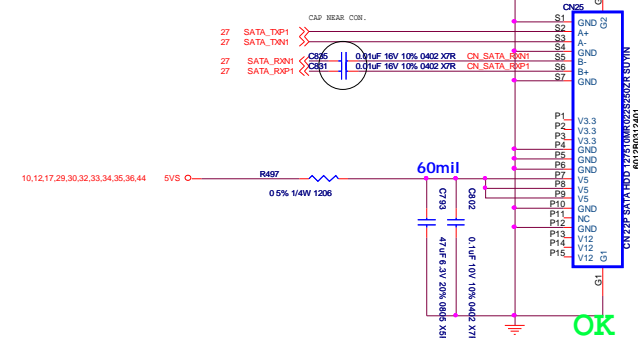
Check BIOS type



LVDS Interface

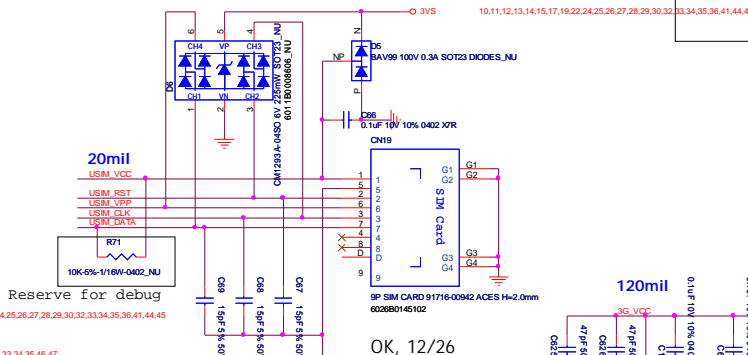


HDD I/F

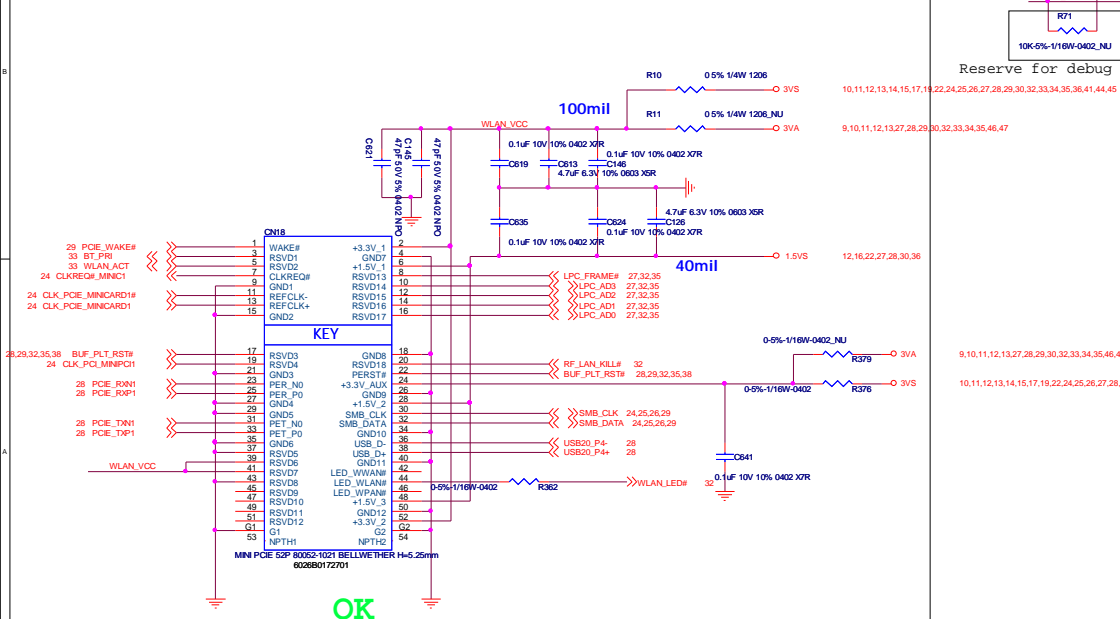


SIM CARD slot

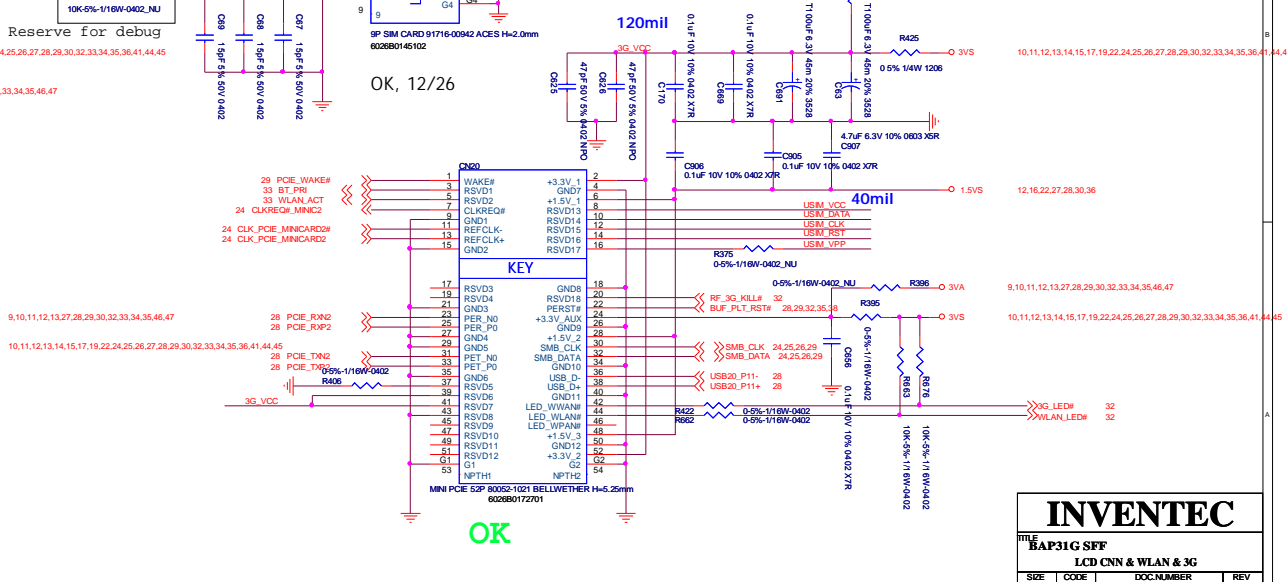
On Chip 5V to 3.3V regulator. No external regulator required
On-Chip power MOSFETs for supplying flash media card power.



PCIE Mini Card(WLAN)

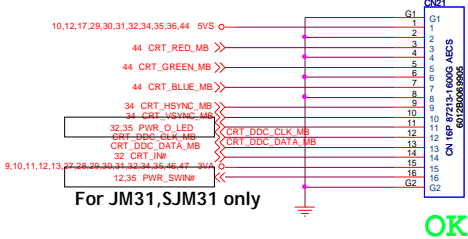


PCIE Mini Card for 3G

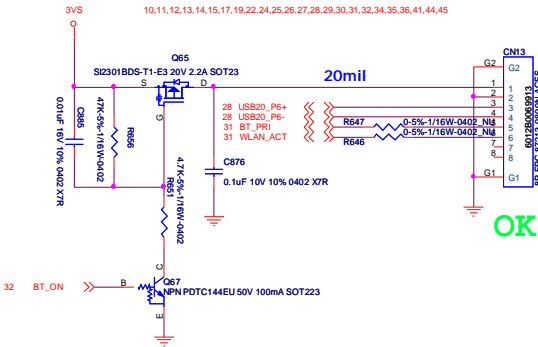


VGA Board CN

(CRT+ PWR SW)

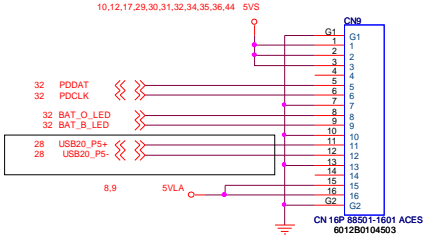


Bluetooth CON.

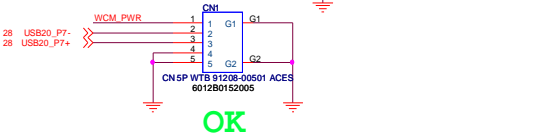


GLIDE PAD Board

For BAP31 only

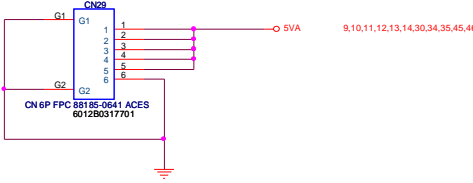
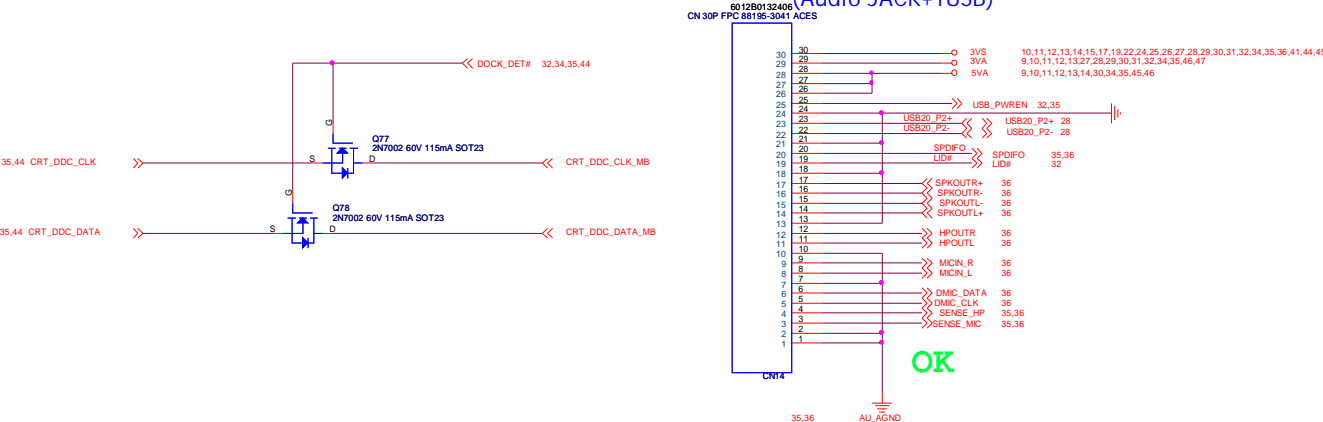


WEB Cam.



AUDIO Board CN

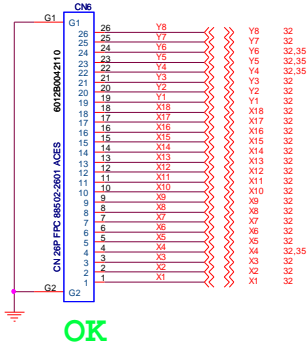
(Audio JACK+1USB)



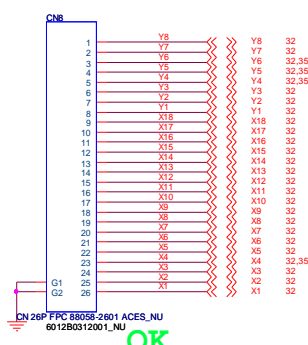
INVENTEC
BAP31G SFF
Daughter Connector

SIZE	CODE	DOC NUMBER	REV
Custom	C3	D-CS-1310A2268501-ALG	A03
SHEET		33	47

To K/B(For All Model)



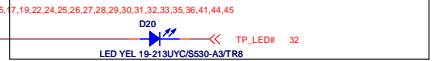
To K/B(No Use)



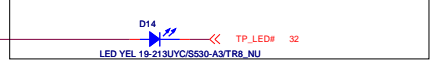
GP lock Button / LED(FOR SJM31)



GP lock Button / LED(FOR BAP31)

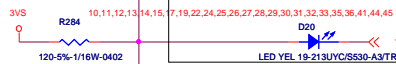


GP lock Button / LED(FOR JM31)

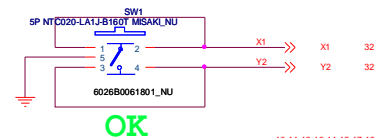


R284

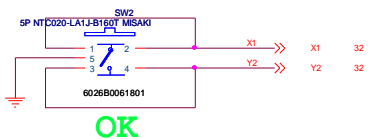
120 ohm for JM31, BAP31
470 ohm for SJM31



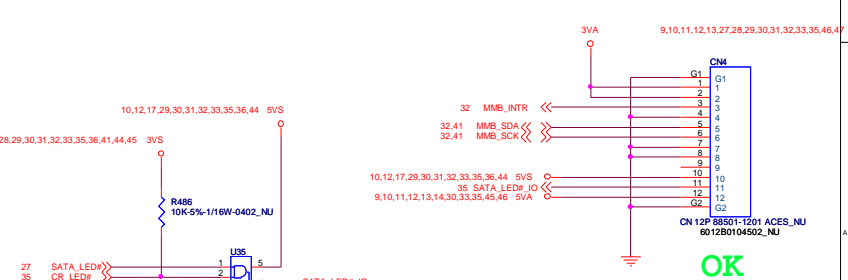
SW (No Use)



SW (FOR All Model)



SW Sensor BOARD(For JM31,SJM31)



INVENTEC

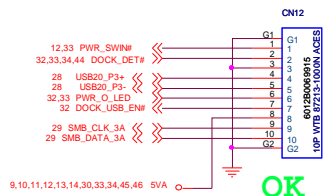
TITLE			
BAP31G SFF			
BDP			
SIZE	CODE	DOC NUMBER	REV
Custom	C3	D-CS-1310A2268501-ALG	A03
SHEET			
34	47		

CHANGE by S.H.Chung DATE Tuesday, May 26, 2009

For BAP31(EASY/B)

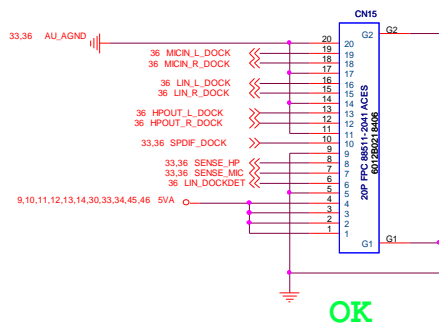
MB(USB) TO EASY/B

For BAP31



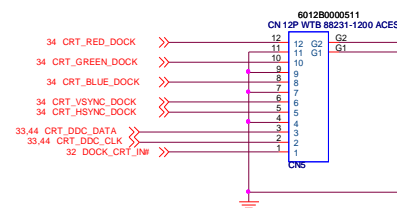
MB(AUDIO) TO EASY/B

For BAP31



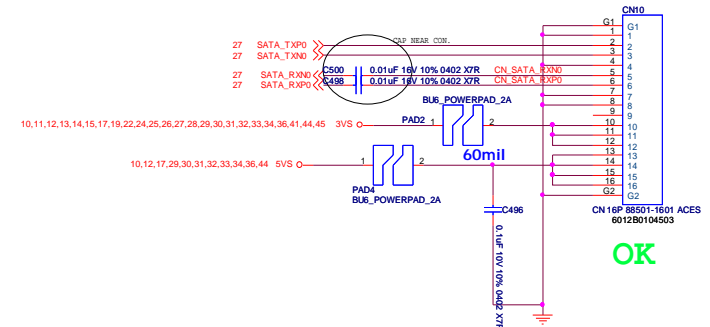
MB(RGB) TO EASY/B

For BAP31

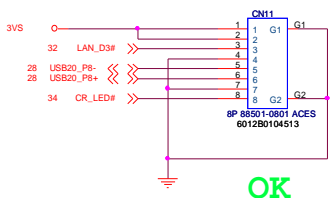


SSD I/F

For All Model

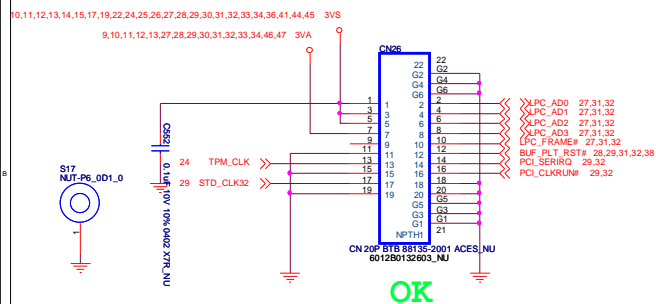


Card Reader BOARD CN
For All Model



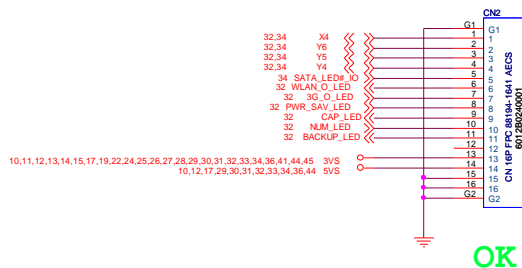
NO NEED

TPM CN

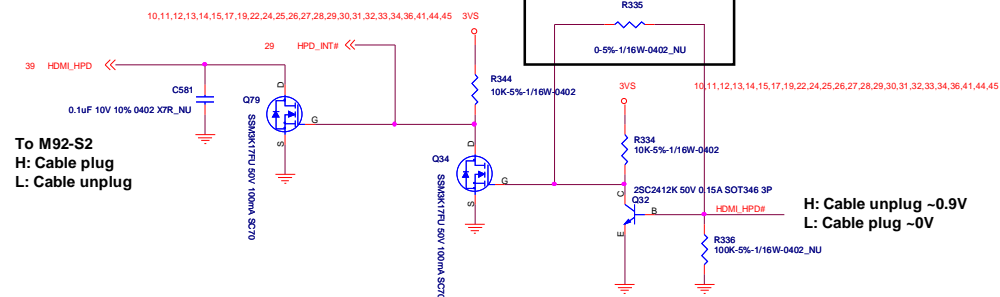


For BAP31

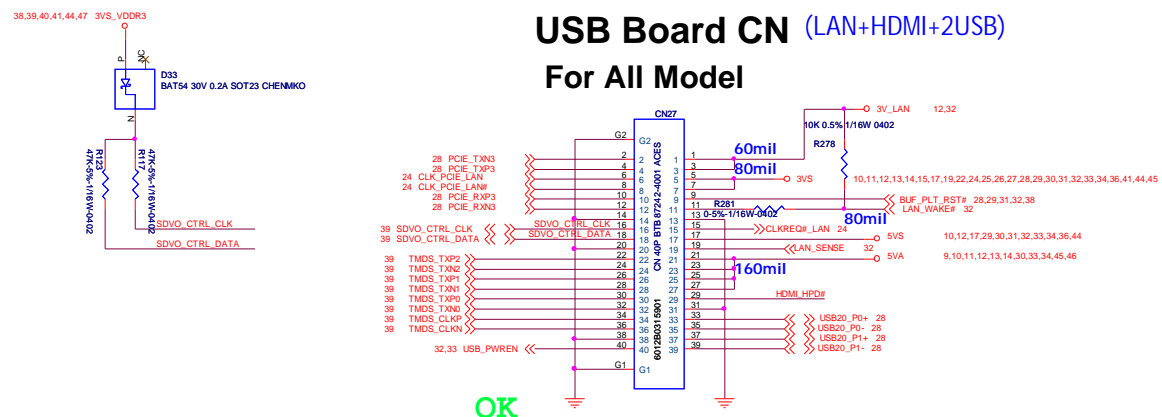
SW/B CN



To ICH-9M
H: Cable unplug
L: Cable plug



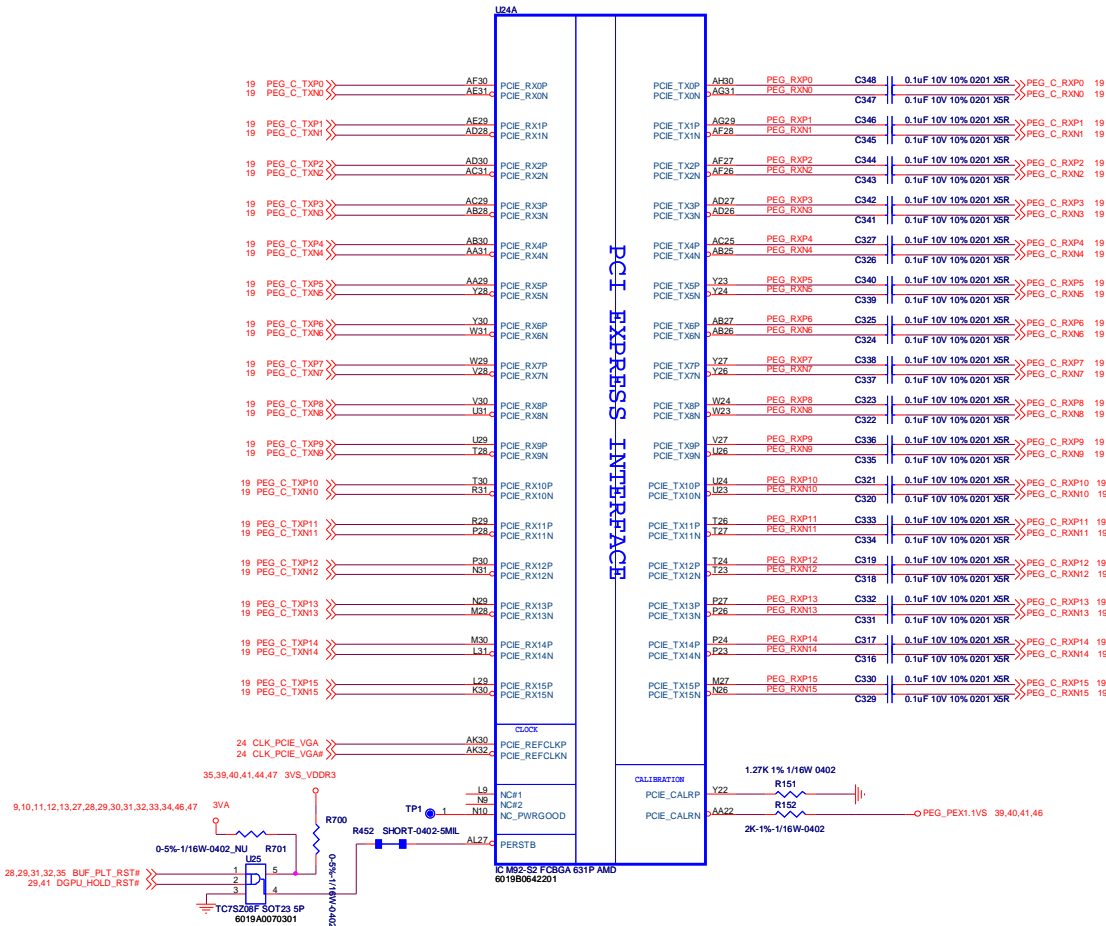
USB Board CN (LAN+HDMI+2USB)
For All Model

**INVENTEC**

TITLE			
BAP31G SFF			
BDP			
SIZE	CODE	DOC. NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03

BLANK

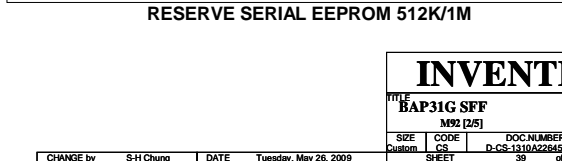
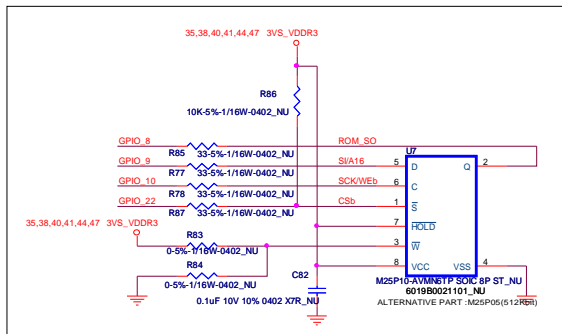
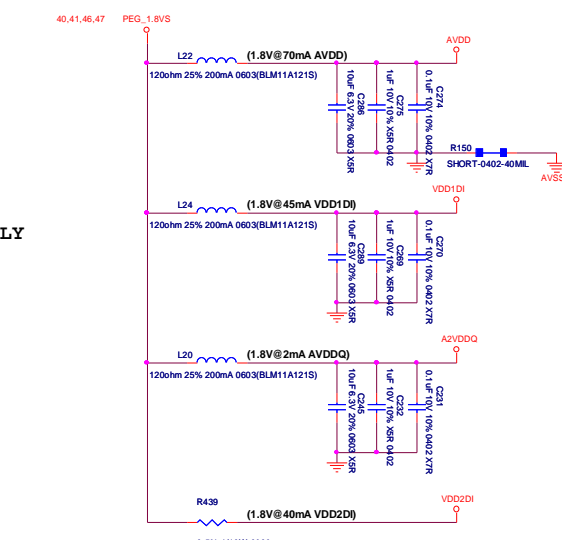
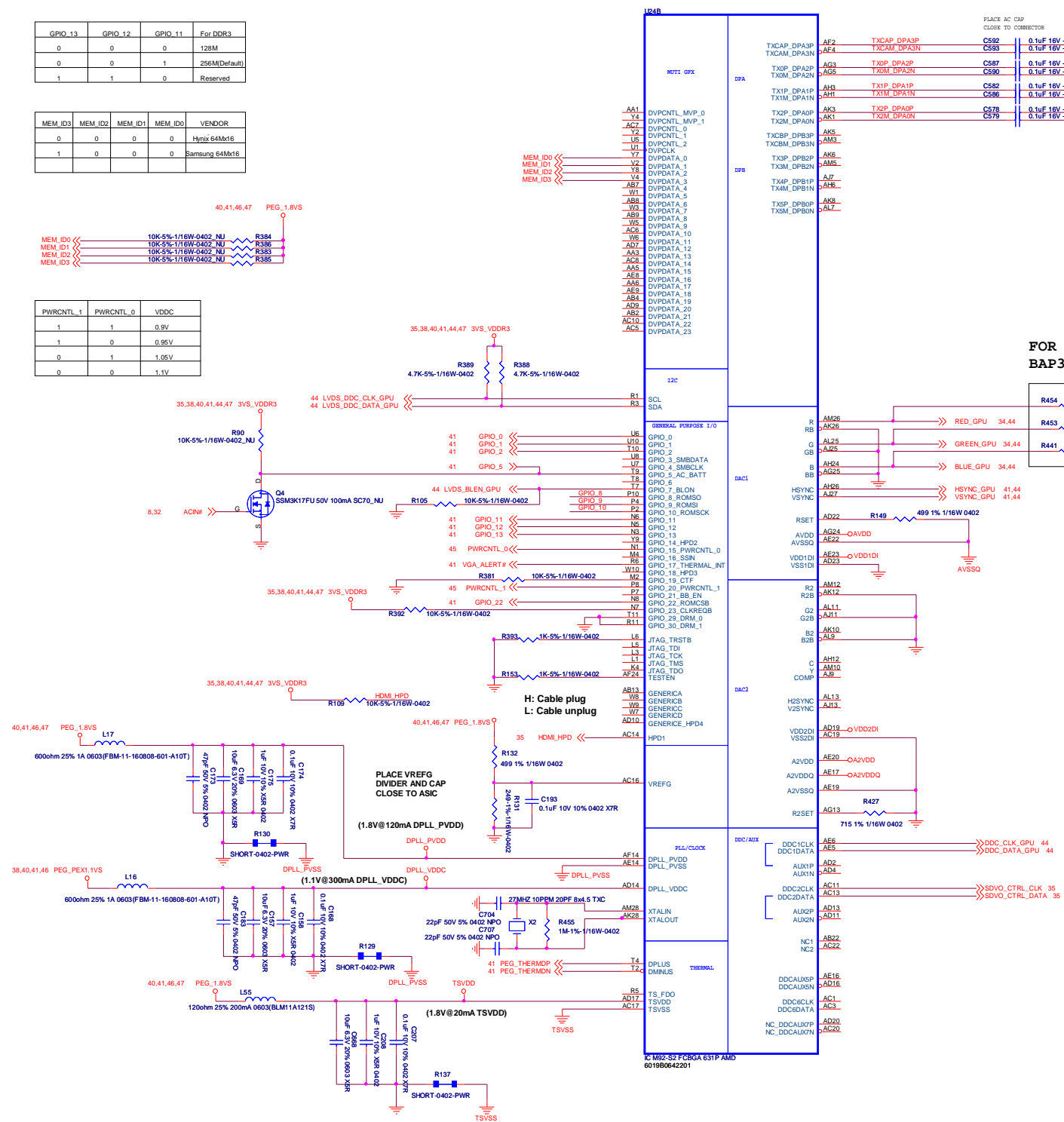
INVENTEC			
TITLE BAP31G SFF BLANK			
SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A224501-ALG	A00



GPIO_13	GPIO_12	GPIO_11	For DDR3
0	0	0	128M
0	0	1	256M(Default)
1	1	0	Reserved

MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	VENDOR
0	0	0	0	Hynix 64Mx16
1	0	0	0	Samsung 64Mx16

PWRCNTL_1	PWRCNTL_0	VDDC
1	1	0.9V
1	0	0.95V
0	1	1.05V
0	0	1.1V



INVENTEC

BAP31G SFF

M92 [2/5]

SIZE

Custom

CODE

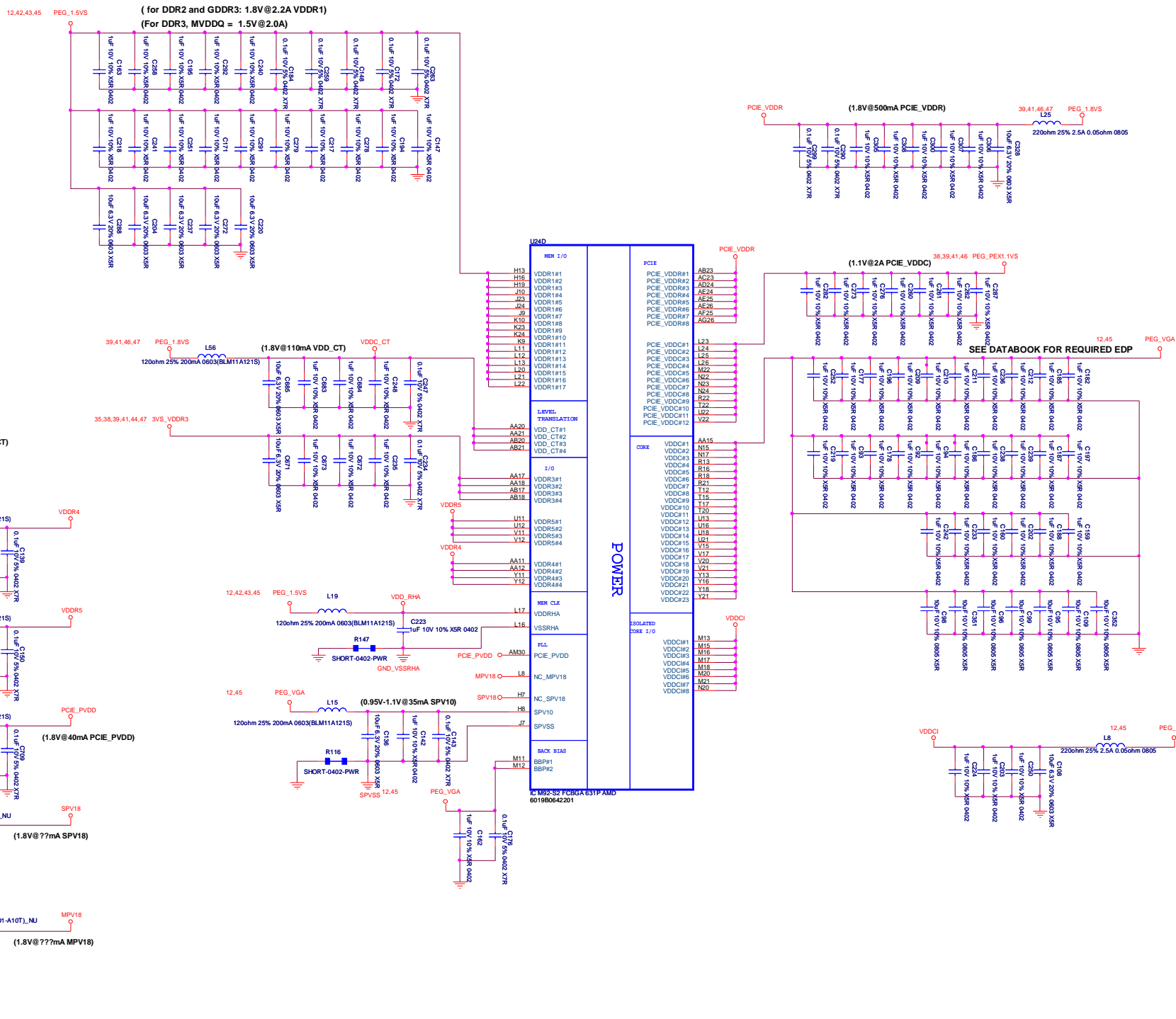
CS

DOCNUMBER

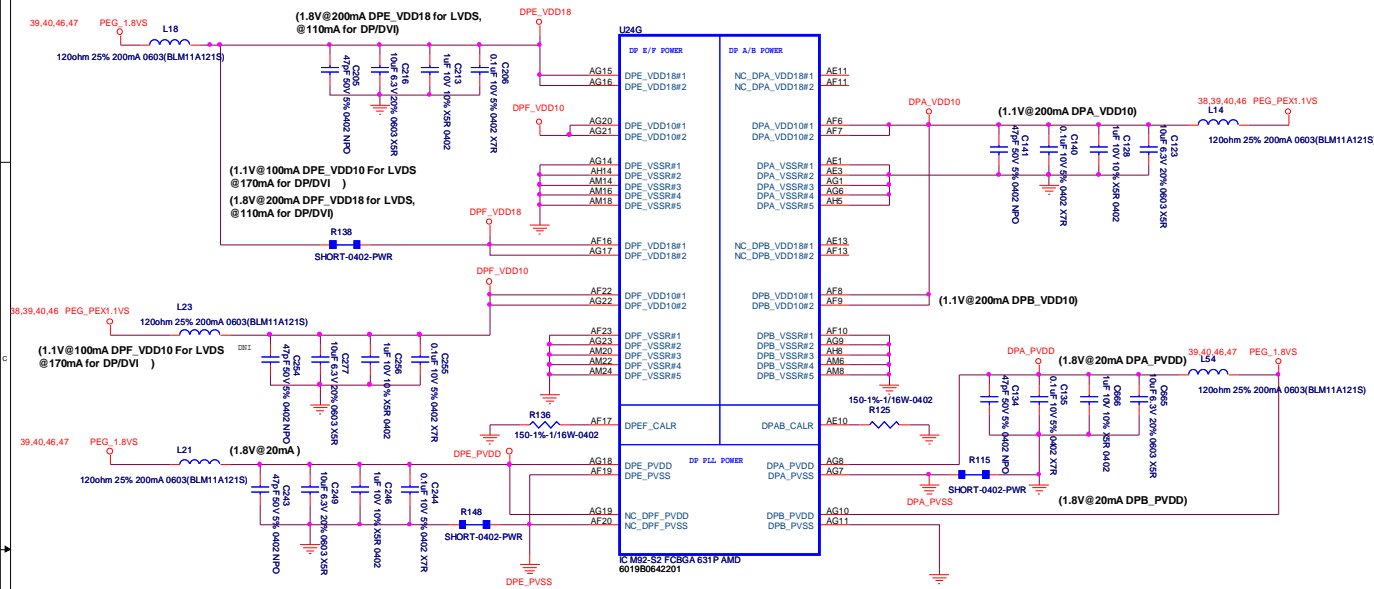
D-CS-1310A2264591-ALG_A03

REV

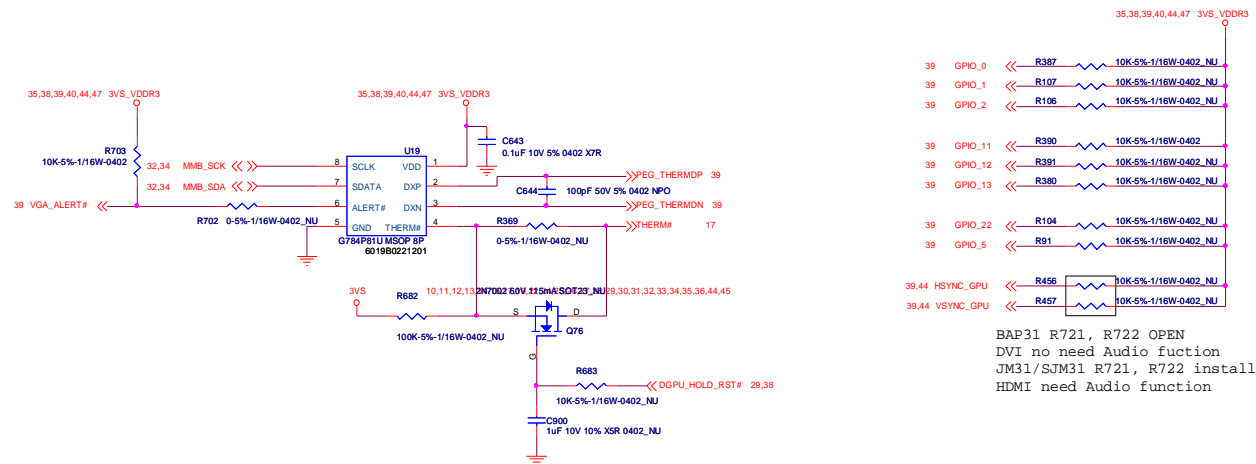
03



For 92, DPx_VDD10 = 1.1V
For Future ASIC, DPx_VDD10 = 1.0V



PIN STRAPS



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

<p>RECOMMENDED SETTINGS</p> <p>0= DO NOT INSTALL RESISTOR</p> <p>1 = INSTALL 10K RESISTOR</p> <p>X = DESIGN DEPENDANT</p> <p>NA = NOT APPLICABLE</p>
--

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERIC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function	X X
		0 1 Audio for DisplayPort and HDMI if dongle is detected	
		1 0 Audio for DisplayPort only	
		1 1 Audio for both DisplayPort and HDMI	

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
<p>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</p>	
GPIO21_BB_EN	

BAP31 R721, R722 OPEN
DVI no need Audio fuction
JM31/SJM31 R721, R722 install
HDMI need Audio function

INVENTEC

TITLE
BAP31G SFF
M92 [4/5]

SIZE	CODE	DOC NUMBER	REV
Custom	CS	D-CS-1310A2264501-ALG	A03
SHEET		41 of	47

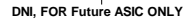
U24C



U2



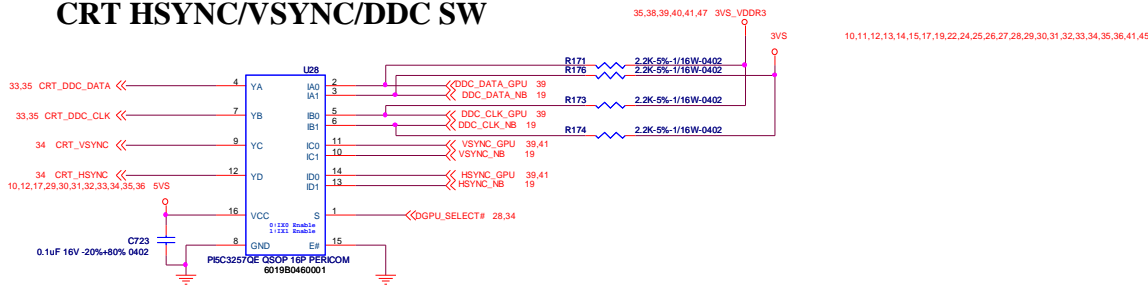
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC



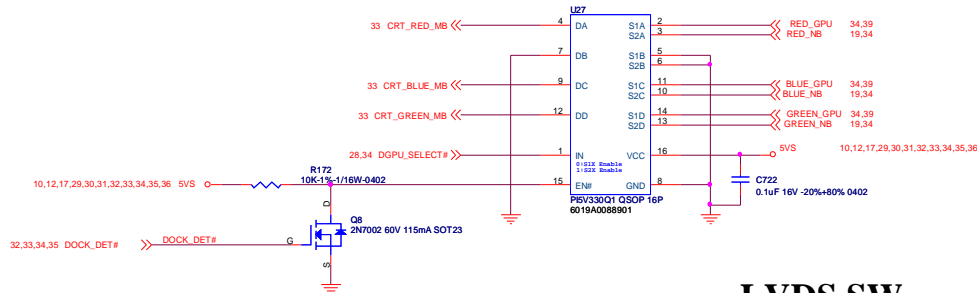
[/WW.AliSaler.Com](http://WW.AliSaler.Com)

CHANGE by	S-H Chung	DATE	Tuesday, May 26, 2009
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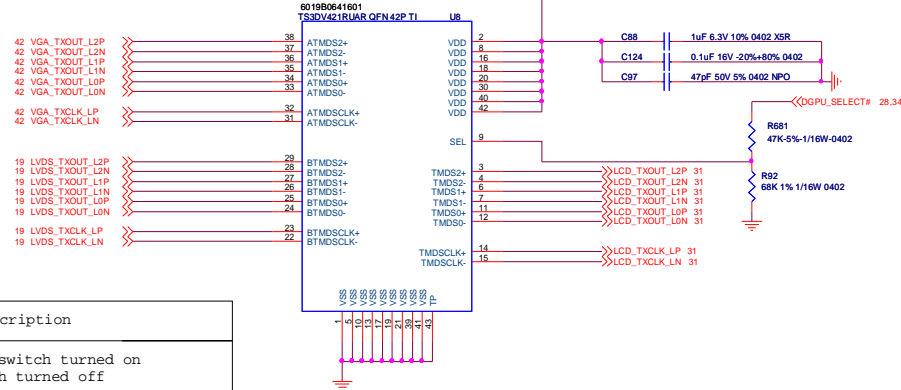
CRT HSYNC/VSNC/DDC SW



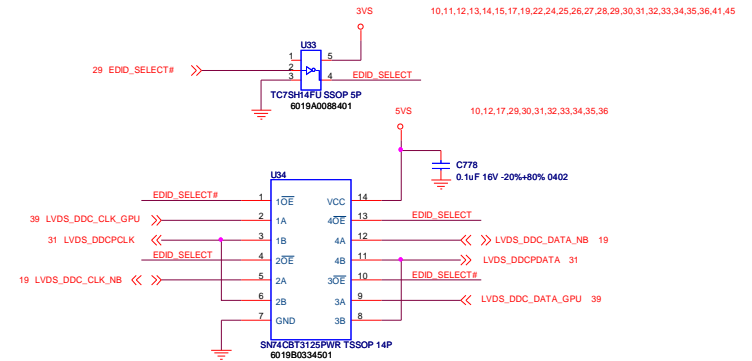
CRT R/G/B SW



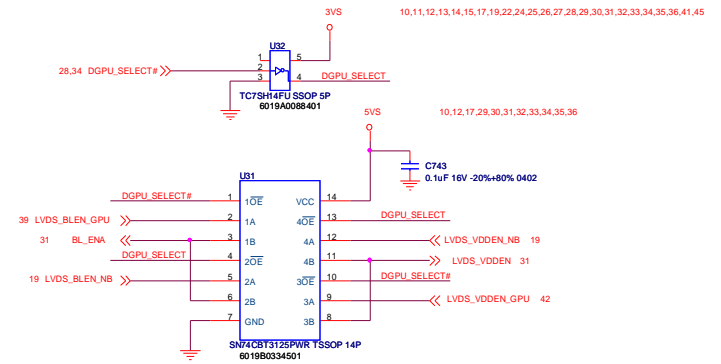
LVDS SW



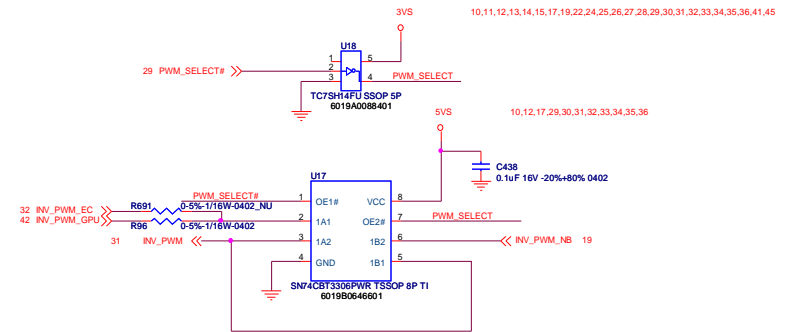
LCD DDC SW



LVDS BKL and Vcc Enable SW



LCD PWM SW



Signal	During Reset	After Reset	Description
DGPU_PWR_EN#	High	High	0 : dGPU power switch turned on 1 : power switch turned off
DGPU_PWROK			0 : dGPU power is not stable 1 : dGPU power is stable
DGPU_HOLD_RST#	Low	Low	0 : Keep dGPU in reset 1 : Reset is released
DGPU_SELECT#	High	High	0 : Display switch enabled for dGPU 1 : Display switch enabled for iGPU
HPD_INT#			0 : DVI insertion 1 : No DVI insertion
PWM_SELECT#		High	0 : PWM switch enabled for dGPU 1 : PWM switch enabled for iGPU
EDID_SELECT#		High	0 : EDID/DDC switch enabled for dGPU 1 : EDID/DDC switch enabled for iGPU

INVENTEC

MLB
BAP31G SFF

Hybrid Switch

SIZE Custom CODE CS SHEET DOCNUMBER D-CS-1310A2264591-ALG_A03 REV 44 9 47

CHANGE by S-H Chung

DATE Tuesday, May 26, 2009

